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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,345	08/18/2003	Noriaki Hiraga	052593-5003-01	3808

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EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,345	HIRAGA, NORIAKI	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20 - 45* is/are pending in the application.

4a) Of the above claim(s) *29, 30, 32 - 35, 37 - 45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20 - 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *31 and 36* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Applicant's election without traverse of Group I, claims 20 – 28, 31 and 36 in the reply filed on February 09, 2005 is acknowledged.

However, Claim 31 is dependent on non-elected Claim 30and Claim 36 is dependent on non-elected Claims 29 and 35. Therefore, Claims 31 and 36 cannot be examined as requested and are subject to further restriction. In the parent case 09/625,643 the Claims 31 and 36 have been selected in other groups (former Groups 4, 5 and 6).

IDS

The information disclosure statement filed on August 18, 2003 regarding reference JP 11-505374 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. Therefore, the reference JP 11-505374 has not been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A reason for that is in the following claim limitation: "said static area includes a partial region of an active element on a transmission side of said active elements in the first connection configuration" (emphasis added). According to Specification (paragraph [0140]), "The inter-circuit auxiliary wire 29 has one end connected directly to the source of the pMOS transistor 12AP in the internal circuit 4A (see FIG. 4B). This source region is a partial region connected to the power line 8A in the internal circuit 4A in the active element 12AP on the transmission side within the active elements in the first connection configuration connected to the inter-circuit signal wire 12". However, according to Fig. 4B, the inter-circuit signal wire (wire 12 in Fig. 4B) is connected to the bottom of the element 12AP, which means that the bottom part of 12AP is the transmission side of the partial region, while the auxiliary wire (wire 29 in Fig. 4B) is connected to the upper part of 12AP. Therefore the auxiliary wire is not connected to the transmission side of the active element. For purpose of examination, a patentable weight is not given to the underlined limitation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda (US 5,828,108) in view of Otomo et al. (US 5,784,235). Regarding Claim 20, Toyoda discloses following elements: the integrated circuit having a plurality of internal circuits (elements 12 and couple of I/O transistors in the upper left corner in Fig.6) arranged internally in a circuit forming region, the internal circuits-having different power lines (elements VDD1 and VDD2 in Fig. 2A and 2B); an inter-circuit signal wire (element 17 in Fig. 6) interconnecting the couple of input transistors with one of the internal circuits; and an inter-circuit auxiliary wire (the wire connecting VDD to the upper left cell 21 in Fig. 6), which in turn is connected to a static area near a location at which said inter-circuit signal wire is connected. The static area is defined by Specification as the area, where an electrical condition does not dynamically change in a normally operating state, i.e. area of the power supply satisfies this limitation. The auxiliary wire carrying VDD is connected to the cell through the first diffused region (element 21 in Fig. 7C) at location at which the inter-circuit signal wire (connection 17 in Fig. 6) is connected to the cell. However, it does not disclose the circuit having different power lines. Otomo et al. disclose the internal circuits having different power lines (V21, V22, V23 and V2n in Fig. 12). Therefore, in the Toyoda circuit modified according to Otomo et al., the gates of the protection elements will be connected to the power lines of the individual circuits. Both references have the same problem solving area, namely protection of the semiconductor circuits against ESD. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Toyoda

solution by adding the feeding of the individual circuits from different power supplies according to Otomo et al., because as Otomo et al. state (col. 1, lines 14 – 24), reduction of power supply voltages in VLSI often requires to use different power supply voltages.

Regarding Claim 21, Toyoda discloses the cells of the integrated circuit as macrocells (col. 1, lines 21 – 27), which inherently have a plurality of basic cells with the active elements regularly arranged in repetition.

Regarding Claim 22, Toyoda discloses a substrate formed in a single chip (shown in Fig. 2B), and the circuit-forming region is allocated to one surface (upper surface) of said substrate.

Regarding Claim 23, Toyoda discloses the signal input/output circuits (couple of I/O transistors in the upper left corner of Fig. 6) outside the internal circuits (elements 12 in Fig. 6), and external connection terminals outside said input/output circuits (element 15 in Fig. 6). As to a plurality of terminals, Otomo et al. disclose a plurality of I/O terminals (elements 10 and 14 in Fig. 9).

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda in view of Otomo et al. and Tan et al. Regarding Claim 24, Toyoda discloses the active elements in the first connection configuration (couple of I/O transistors in the upper left corner in Fig. 6) connected to the inter-circuit signal wire (element 17 in Fig. 6) and the static area (area 21 in Fig. 6 and 7C) including a partial region of an active element on a transmission side of the active elements in the first connection configuration. Otomo et

al. disclose the static area (area 21 in Fig. 6 and 7C) including a partial region of an active element (elements 132 in Fig. 11). However, it does not disclose an active element in the second connection configuration. As to an active element in the second connection configuration, it is disclosed by Tan et al. in Fig. 3, wherein the additional ESD protection Circuitry (element 170) protects the internal circuit (element 110 in Fig. 3) from ESD events on power supply line Vdd. Tan et al. further disclose the gates of the active element in the second connection configuration being connected only to power lines (element 170 in Fig. 3 is the element with the second connection configuration) and being isolated from signal wires other than said inter-circuit auxiliary wire (Vdd). Both references have the same problem solving area, namely providing ESD protection for semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Toyoda solution by adding the protection element according to Tan et al., because as Tan et al., state (col. 1,lines 17 – 22, col. 1, line 53 – col. 2, line 11), the semiconductor devices are to be protected against ESD events.

Regarding Claim 25, Tan et al. disclose a plurality of the active elements in the second connection configuration (elements 130A in Fig. 7). As to their position relative to the protected circuit, Examiner takes an Official Notice that positioning the ESD protection elements in close proximity to the protected circuit is a common practice. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Tan et al. solution by placing both protection elements arranged in the first and the second connection configurations as

close as possible to the protected cell (surrounding the protected cell), because it reduces parasitic resistances and capacitances thus reducing a propagation delay in the ESD protection act.

Regarding Claim 26, Toyoda discloses the cells of the integrated circuit as macrocells (col. 1, lines 21 – 27), which inherently have a plurality of basic cells with the active elements regularly arranged in repetition.

Regarding Claim 27, Toyoda discloses a substrate formed in a single chip (shown in Fig. 2B), and the circuit-forming region is allocated to one surface (upper surface) of said substrate.

Regarding Claim 28, Toyoda discloses the signal input/output circuits (couple of I/O transistors in the upper left corner of Fig. 6) outside the internal circuits (elements 12 in Fig. 6), and external connection terminals outside said input/output circuits (element 15 in Fig. 6). As to a plurality of terminals, Otomo et al. disclose a plurality of I/O terminals (elements 10 and 14 in Fig. 9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

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